BQ25798 I2C Controlled, 1- to 4-Cell, 5-A Buck-Boost Battery Charger with MPPT for Solar Panels

by Startobytes

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Version 2.0

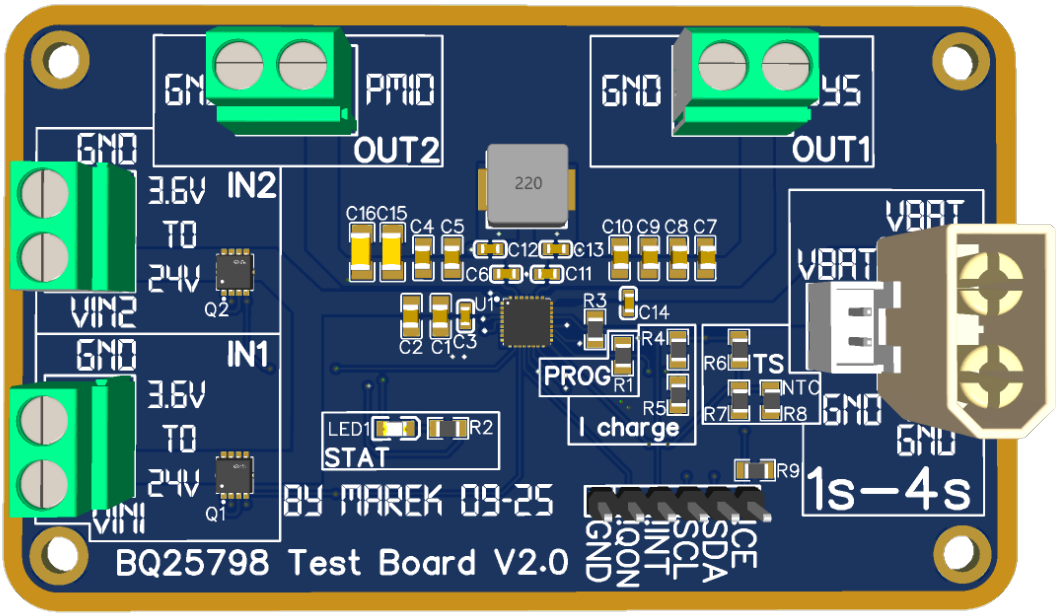

Table of Content

1 Introduction

The BQ25798 is a highly integrated battery charge management IC that supports multiple input sources, including solar panels and USB. It features advanced Maximum Power Point Tracking (MPPT), programmable charging profiles, and I^2C communication for control and monitoring.

2 System Overview

- **Input Sources:** USB, Solar panel, Adapter
- **Battery Types:** 1–4 cell Li-ion, Li-polymer
- **Features:** MPPT, JEITA support, I^2C programmable, input current optimization

3 Battery Charging Configuration

3.1 Charging Profiles

3.1.1 PROG Pin Configuration

At POR, the charger detects the PROG pin pull-down resistance, then sets the charger default POR switching frequency and the battery cell count. Follow the resistance list in Table 1 to set the desired POR switching frequency and battery cell count. The surface mount resistor with ±1% or ±2% tolerance is recommended.

Switching Frequency	Cell Count	Typical Resistance at Prog Pin
1.5 MHz	1s	3.0 kΩ
750 kHz	1s	4.7 kΩ
1.5 MHz	2s	6.04 kΩ
750 kHz	2s	8.2 kΩ
1.5 MHz	3s	10.5 kΩ
750 kHz	3s	13.7 kΩ
1.5 MHz	4s	17.4 kΩ
750 kHz	4s	27.0 kΩ

Table 1: PROG Pin Resistance to Set Default Switching Frequency and Battery Cell Count (as seen in the BQ25798 datasheet [1, p. 46])

3.1.2 Dulal Vbus Inputs

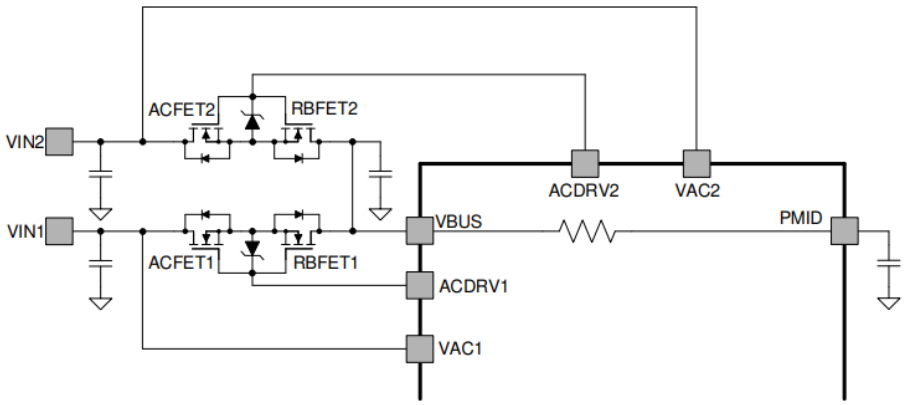

Figure 1: Dual Input Connected to VBUS With ACFET-RBFET (as seen in the BQ25798 datasheet [1, p. 46])

PIN OR REGISTER FIELD	STATE
External MOSFETs	ACFET1, RBFET1, ACFET2, RBFET2
VAC1 pin	Connected to input source 1
VAC2 pin	Connected to input source 2
ACDRV1 pin	Connected to ACFET1/RBFET1 gate terminals
ACDRV2 pin	Connected to ACFET2/RBFET2 gate terminals
ACRB1_STAT	0: ACFET1/RBFET1 Open (Path Disabled)
	1: ACFET1/RBFET1 Closed (Path Enabled)
ACRB2_STAT	0: ACFET2/RBFET2 Open (Path Disabled)
	1: ACFET2/RBFET2 Closed (Path Enabled)
DIS_ACDRV	0: Allow ACDRV1 or ACDRV2 on if all requirements met
	1: Force ACDRV1 and ACDRV2 off
EN_ACDRV1	0: Force ACDRV1 Off
	1: Turn ACDRV1 On if all requirements met
EN_ACDRV2	0: Force ACDRV2 Off
	1: Turn ACDRV2 On if all requirements met

Table 2: Dual Input Configuration Summary (as seen in the BQ25798 datasheet [1, p. 46])

OTG Temperature Limits

During OTG mode, the temperature must stay between:

- **TBCOLD**: -10°C
- **TBHOT**: 60°C

If outside this range, OTG is suspended until the temperature recovers.

Integrated ADC

A 16-bit ADC monitors key system voltages and currents:

- Channels include: IBUS, IBAT, VBUS, VPMID, VBAT, VSYS, TS, TDIE
- Supports one-shot or continuous sampling
- ADC can be disabled to save power

Programmable Features

The charger allows programmable control for:

- Charge current and voltage in each temperature zone
- JEITA thresholds via TS_COOL and TS_WARM registers
- Fault reporting and interrupt masking

4 Maximum Power Point Tracking for Small PV Panel

The charger includes a built-in algorithm to maximize the power drawn from a solar panel. This is known as Maximum Power Point Tracking (MPPT). The power output of a solar panel depends mainly on sunlight and temperature. Its maximum power point is usually found about 70%–90% of its open-circuit voltage (VOC). The charger automatically and regularly measures the VOC from the input source and sets the input voltage regulation point (VINDPM) to a ratio of this value. To make MPPT effective, it is recommended to set the charging current to the highest allowed value so that VINDPM remains active. MPPT is off by default after power-up (`EN_MPPT = 0`) and only starts when `EN_MPPT` is set to 1. If the battery voltage is too low (below `VSYSMIN`), MPPT cannot be enabled, and any attempt to set `EN_MPPT` to 1 will be ignored and reset to 0. During MPPT operation, the charger briefly stops switching to measure the VOC at the input (VBUS). During this time, the system runs on battery power. The charger then updates VINDPM to `VOC_PCT[2:0]` × VOC. This cycle repeats with timing controlled by `VOC_DLY[1:0]` and `VOC_RATE[1:0]`. If the input voltage drops below `VBUS_PRESENT`, MPPT is turned off and cannot be re-enabled until the input returns. Only one of the following features can be active at a time: `EN_ICO`, `FORCE_VINDPM_DET`, or `EN_MPPT`. If one is set, the others are blocked until the first is cleared.

5 Component Selection

5.1 Resistors

A **4.7 kΩ** resistor was used to set the voltage at **1S** and the switching frequency at **750 kHz** as shown in Table 1. The selected component is a 125 mW thick film resistor rated at 150 V, with a tolerance of **±1%** and a temperature coefficient of ±100 ppm/°C. It is a **4.7 kΩ, 0805** surface-mount (SMD) chip resistor, compliant with RoHS.

5.2 Inductor Selection

The device offers a 1.5MHz switching frequency for compact designs using 1µH inductors and small capacitors, and a 750kHz option for higher efficiency with 2.2µH inductors and larger capacitors. Each frequency must be used with its corresponding inductor value.

Switching frequency	Inductor value
750kHz	2.2µH
1.5MHz	1µH

Table 3: Inductor Selection Table (as seen in the BQ25798 datasheet [1, p. 46])

Since the converter can operate in either buck or boost mode, the inductor current equals either the charging current or the input current. The inductor's saturation current must exceed the greater of the input current (I_{in}) or charging current (I_{chg}) plus half the ripple current (I_{ripple}).

$$I_{\mathrm{SAT}} \geq \max\left[\left(I_{\mathrm{IN}} + \frac{I_{\mathrm{RIPPLE}}}{2}\right), \left(I_{\mathrm{CHG}} + \frac{I_{\mathrm{RIPPLE}}}{2}\right)\right] \tag{1}$$

The inductor ripple current (I_{ripple}) depends on the input voltage (V_{bus}), the output voltage (V_{sys}), the switching frequency (F_{sw}), and the inductance (L). The inductor current ripples for buck mode and boost mode are calculated with Equation 2 and Equation 3, respectively:

$$I_{\mathrm{RIPPLE\_BUCK}} = \frac{V_{\mathrm{SYS}} \times (V_{\mathrm{BUS}} - V_{\mathrm{SYS}})}{V_{\mathrm{BUS}} \times F_{\mathrm{SW}} \times L} \tag{2}$$

$$I_{\mathrm{RIPPLE\_BOOST}} = \frac{V_{\mathrm{SYS}} \times (V_{\mathrm{SYS}} - V_{\mathrm{BUS}})}{V_{\mathrm{SYS}} \times F_{\mathrm{SW}} \times L} \tag{3}$$

5.2.1 selected Inductor

The selected component is a **2.2 μH** molded power inductor with a **9.5 A** saturation current and a **10 A** rated current. It features a tolerance of ± 20% inductance and comes in a compact **7 × 6.6 mm** surface-mount (SMD) package.

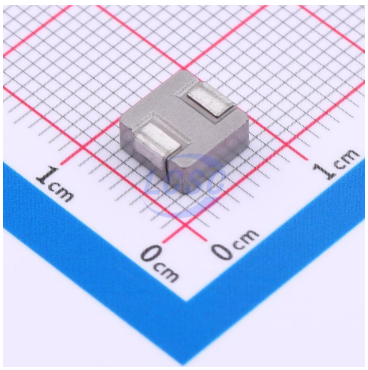

Figure 2: Selected Inductor: C5349701

5.3 Copper Trace Width

This trace must carry **5 A** of current across a **2 cm** length using copper that is **1 oz/ft²** thick. The design limits the rise of the temperature to **20,°C** above an ambient temperature of **25 °C** giving us a maximum trace temperature of **45,°C**. These values are critical because when current flows through a conductor, such as a PCB trace, it generates heat due to resistance. The trace width must be sufficient to allow that heat to dissipate without exceeding the 20 °C rise. If the trace is too narrow, it could overheat, leading to performance issues or even failure. The copper thickness helps reduce resistance and spread heat, and the trace length contributes to overall resistance, though width is typically the primary design variable calculated based on these inputs. Based on this analysis, the required trace width is approximately **1.82 mm** to ensure safe operation.

Figure 3: Calculated trace width

All calculations are seen in Figure 3 where made with the DigiKey PCB Trace Width Calculator.

5.4 Capacitors

5.4.1 Input Capacitors

In buck mode, the input current is discontinuous, causing the input ripple current and voltage ripple. Input capacitors must handle the ripple current and have enough capacitance to keep voltage ripple low. The input RMS ripple current and voltage ripple depend on the duty cycle $D = \frac{V_{SYS}}{V_{BUS}}$, with the worst case at $D = 0.5$. For a 2-cell battery system

(8 V), this worst case occurs when the input voltage V_{BUS} is between 15 V and 20 V. Use low ESR ceramic capacitors (X7R or X5R) placed near the IC's PMID and GND pins. The capacitor voltage rating should exceed the input voltage; **25 V** or higher is recommended for up to 20 V input. For up to 3.3 A input current, use **one 0.1 μF** plus **three 10 μF** ceramic capacitors. The PMID capacitor also supports voltage stability during backup mode transitions when the adapter is removed. For backup mode, add two **33 μF** POSCAP capacitors at PMID.

5.4.2 Used Capacitors

Three **10 μF**, **25 V** ceramic capacitors were used at the input, following the datasheet recommendations. Ceramic capacitors are preferred over electrolytics due to their superior performance at high frequencies and lower ESR, which makes them more effective at filtering high-frequency ripple. This ensures better input voltage stability and supports the required input RMS current.

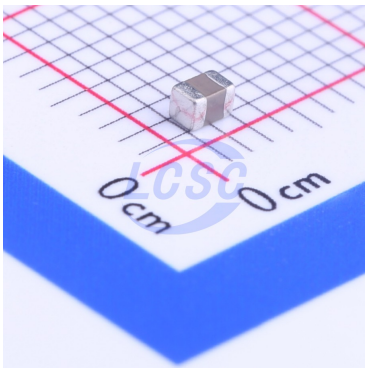

Figure 4: 10 μF ceramic capacitor

6 Pin configurations

6.1 SDRV connection

When a ship FET is not used in the system design, the **SDRV (Ship FET Gate Driver)** pin must be properly terminated to prevent it from floating and to maintain stable system behavior. The SDRV pin is typically used to drive the gate of an external N-channel MOSFET used for ship mode functionality.
In the absence of a ship FET, it is recommended to connect a **1nF**, **50V** rated ceramic capacitor between **SDRV** and **BAT**. The capacitor should be in a **0603** package.
This configuration complies with datasheet guidance for unused ship FET cases and ensures reliable pin behavior during mode transitions.

6.2 ILIM HIZ Pin

The **ILIM_HIZ** pin is used to program the input current limit and also controls a HiZ-like operating mode. The pin is configured using a resistor divider from a pull-up rail to ground, with the midpoint connected to the ILIM_HIZ pin.
The voltage at the ILIM_HIZ pin is calculated using the equation:

$$V_{\text{ILIM\_HIZ}} = 1\,\text{V} + 800\,\text{m}\Omega \times I_{\text{INDPM}} \tag{4}$$

$$I_{\text{INDPM}} = \frac{V_{\text{ILIM\_HIZ}} - 1\,\text{V}}{800\,\text{m}\Omega} \tag{5}$$

where I_{INDPM} is the target input current.
The actual input current limit used by the charger is the lower of the ILIM_HIZ pin setting and the value programmed into the `IINDPM` register.
If $V_{\text{ILIM\_HIZ}} < 0.75\,\text{V}$, the buck-boost converter enters a non-switching mode (HiZ-like behavior), similar to setting the `EN_HIZ` bit, but with the `REGN` LDO remains active. When $V_{\text{ILIM\_HIZ}} > 1\,\text{V}$, the normal switching operation resumes.
To configure the charger for maximum input current limit, connect the ILIM_HIZ pin directly to `REGN`.

6.2.1 Current Setting

To set the desired input current limit I_{INDPM} using a resistor divider connected between a 5V pull-up rail and ground, the voltage at the ILIM_HIZ pin is determined by both the input current and the resistor ratio.
First, compute the ILIM_HIZ voltage based on the target current:

$$V_{\text{ILIM\_HIZ}} = 1\,\text{V} + 0.8\,\Omega \cdot I_{\text{INDPM}} \tag{6}$$

This voltage is set by the resistor divider:

$$V_{\text{ILIM\_HIZ}} = 5\,\text{V} \cdot \frac{R_2}{R_1 + R_2} \tag{7}$$

Solving for the resistor ratio as a function of the target current:

$$\frac{R_1}{R_2} = \frac{5}{1 + 0.8 \cdot I_{\text{INDPM}}} - 1 \tag{8}$$

For a target input current limit of $I_{\text{INDPM}} = 1.0\,\text{A}$ (1000 mA), With the actual component values used—$R_2 = 10\,\text{k}\Omega$ and $R_1 = 18\,\text{k}\Omega$—the calculated current limit is approximately 975 mA, according to the resistor divider equation:

$$\frac{R_1}{R_2} = \frac{5}{1 + 0.8 \times 1.0A} - 1 = \frac{5}{1 + 0.8} - 1 = \frac{5}{1.8} - 1 \approx 1.77 \tag{9}$$

Choosing $R_2 = 10\,\text{k}\Omega$, then

$$R_1 = 1.77 \times 10\,\text{k}\Omega = 17.7\,\text{k}\Omega \approx \mathbf{18k\Omega} \tag{10}$$

Solving for I_{INDPM} with the given resistor values:

$$I_{\text{INDPM}} = \frac{\left(\frac{R_2}{R_1+R_2} \cdot 5\right) - 1}{0.8} \approx 0.975\,\text{A} = 975\,\text{mA} \tag{11}$$

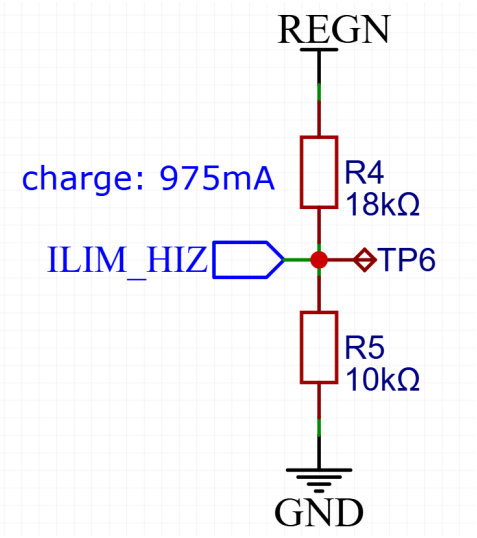

Figure 5: Indpm Voltage Devider

6.3 REGN (Internal Linear Regulator Output)

The **REGN** pin provides the output of the internal linear regulator (LDO) of the charger. It is internally powered from the higher of either **VBUS** or **BAT**. The REGN output supplies the gate drive voltage for internal MOSFETs and serves as the voltage bias for the resistor divider connected to the **TS** (Temperature Sense) pin.
A ceramic capacitor rated 4.7uF, 10V must be connected between **REGN** and power ground. This capacitor is required for LDO stability and proper operation and should be placed close to the REGN pin.

6.3.1 REGN LDO Output Characteristics

Condition	Min (V)	Typical (V)	Max (V)
$V_{BUS} = 5\,V$, $I_{REGN} = 20\,mA$	4.6	4.8	5.0
$V_{BUS} = 15\,V$, $I_{REGN} = 20\,mA$	4.8	5.0	5.2
Current limit at $V_{BUS} = 5\,V$, $V_{REGN} = 4.5\,V$			30 mA typical

Table 4: REGN LDO Output Characteristics (as seen in the BQ25798 datasheet [1, p. 46])

6.4 TS Resistor Network Design

The BQ25798 charger IC uses a TS (thermistor sense) pin to monitor battery temperature via a resistor network. This network typically includes an NTC thermistor and two external resistors: RT1 and RT2.

JEITA Compliance

To comply with JEITA safety standards for Li-ion batteries:

- Charging is suspended if TS voltage is outside the T1–T5 range.

- In the T1–T2 (cool) zone, charging current is reduced to 20%, 40%, or 100% of normal (T2–T3), or suspended.
- In the T3–T5 (warm) zone, charge voltage is reduced by an offset (0 to 800 mV), and current can be limited.

Charge Termination

Termination current is not adjusted by temperature. If reduced current is below the set termination value and battery voltage is within range, charging stops.

6.4.1 TS Resistor Network

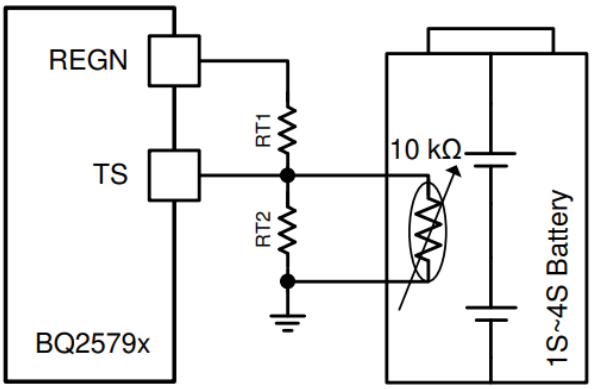

Figure 6: TS Resistor Network (BQ25798 datasheet [1, p. 46])

Found RTH values for NTC as in the LUT of Datasheet of NTC.
(C51597 NTC datasheet [2, p. 46])

$$R_{\text{TH,COLD}} = \mathbf{32.116k}\,\Omega \text{ @ } 0°\text{C}$$
$$R_{\text{TH,HOT}} = \mathbf{2.457k}\,\Omega \text{ @ } 60°\text{C}$$

This is based on a 103AT NTC thermistor and temperature thresholds T1 = 0°C, T5 = 60°C. (as seen in the BQ25798 datasheet [1, p. 46])
$V_{\text{REGN}} = 5\text{V}$(based on [1, p. 16]). Then:

$$VT1 = 73.3\% \cdot V_{\text{REGN}} = \mathbf{3.665}\ \text{V}$$
$$VT5 = 34.2\% \cdot V_{\text{REGN}} = \mathbf{1.71}\ \text{V}$$

(based on [1, p. 14-15]).

The following formulas were derived using the loaded voltage divider formula and a system of equations as shown below.

6.4.2 Equation for R2 parallel NTC and Vout

$$R_{2\|\mathrm{NTC}} = \frac{R_2\, R_{\mathrm{NTC}}}{R_2 + R_{\mathrm{NTC}}} \tag{12}$$

$$V_{\mathrm{out}} = V_{CC}\, \frac{R_{2\|\mathrm{NTC}}}{R_1 + R_{2\|\mathrm{NTC}}} \tag{13}$$

6.4.3 Hot and Cold R2 Equations

$$R_{2,\mathrm{hot}} = \frac{R_2\, R_{\mathrm{hot}}}{R_2 + R_{\mathrm{hot}}} \tag{14}$$

$$R_{2,\mathrm{cold}} = \frac{R_2\, R_{\mathrm{cold}}}{R_2 + R_{\mathrm{cold}}} \tag{15}$$

6.4.4 Solving for R1 from Hot and Cold Voltages (E24)

Condition:

$$R_{1,\mathrm{hot}} = R_{1,\mathrm{cold}} \tag{16}$$

Chosen standard value:

$$R_{T2} \approx \mathbf{4.3\,k\Omega} \tag{17}$$

6.4.5 Hot and Cold R1 Equations

$$R_{1,\mathrm{hot}} = \frac{R_1\, R_{\mathrm{hot}}}{R_1 + R_{\mathrm{hot}}} \tag{18}$$

$$R_{1,\mathrm{cold}} = \frac{R_1\, R_{\mathrm{cold}}}{R_1 + R_{\mathrm{cold}}} \tag{19}$$

6.4.6 Solving for R1

Condition:

$$R_{2,\mathrm{hot}} = R_{2,\mathrm{cold}} \tag{20}$$

Chosen standard value:

$$R_{T1} \approx \mathbf{18\,k\Omega} \tag{21}$$

6.4.7 Minimum and Maximum Output Voltages

$$V_{\mathrm{out,hot}} = V_{CC} \frac{R_{2,\mathrm{hot}}}{R_1 + R_{2,\mathrm{hot}}} \tag{22}$$

$$V_{\mathrm{out,cold}} = V_{CC} \frac{R_{2,\mathrm{cold}}}{R_1 + R_{2,\mathrm{cold}}} \tag{23}$$

6.4.8 Dirived formulas for RT1 and RT2

$$R_{T1} = \frac{ntchot\ ntcold\ (v_1 - v_2)\ v_{cc}}{(ntchot - ntcold)\ v_1\ v_2} \tag{24}$$

$$R_{T2} = \frac{ntchot\ (v_1 - v_{cc})\ v_2 - ntcold\ v_1\ (v_2 - v_{cc})}{(ntchot - ntcold)\ v_1\ v_2} \tag{25}$$

Using Equation 24 and Equation 25, the values of R_{T1} and R_{T2} are calculated as follows: These resistances provide the proper threshold voltages for the TS pin of the BQ25798 according to the datasheet [1, p. 14-15].

Using these values, we can calculate the minimum and maximum Voltages at the Input of the BQ25798.

Figure 7: Minimum and Maximum Voltages for RT1 RT2

The graph shown in Figure 7 displays the acceptable range for the TS pin on the BQ25798 chip to charge the battery where Vin is the REGN Voltage v2calc is the upper Voltage limit and v1calc is the lower voltage limit. All voltages shown in Figure 7 were calculated using "RT1,RT2 calculation Vout.ggb".

7 PCB Component placement

This section shows the placement of all components on the PCB. Figure 8 illustrates the layout of the BQ25798 test board with MPPT for solar applications.

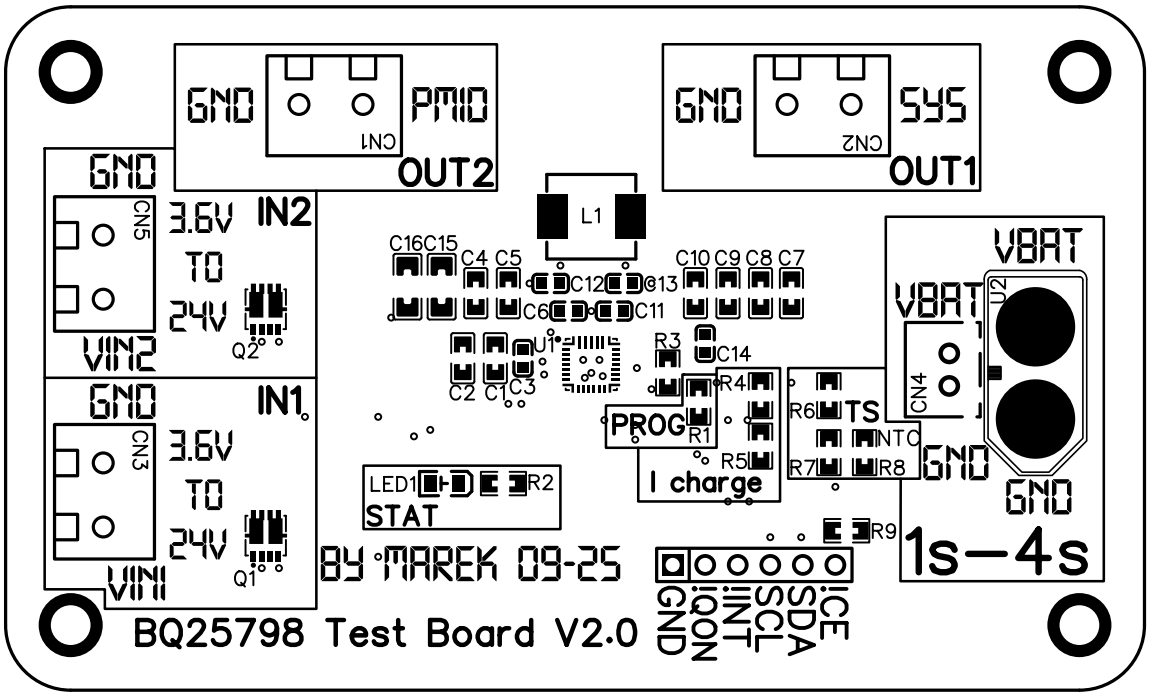

Figure 8: PCB BQ25798 Test Board MPPT Solar

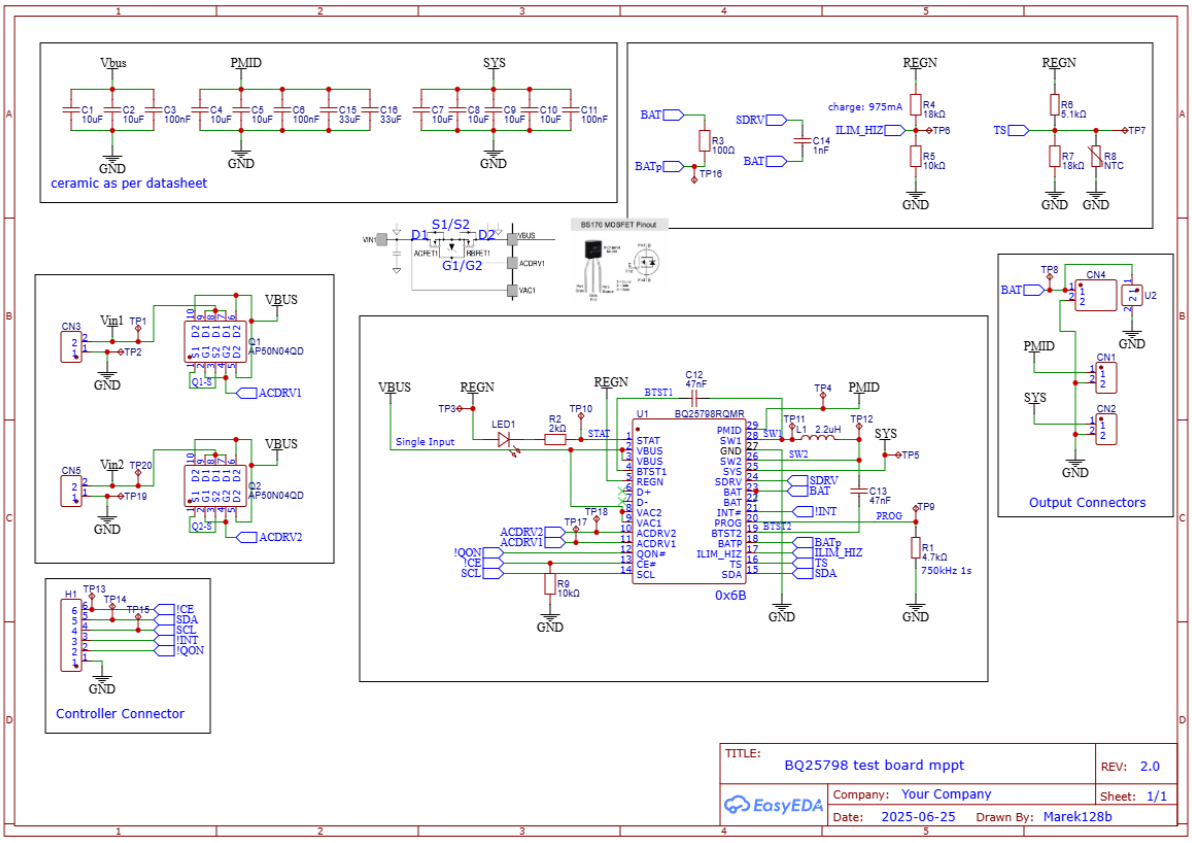

Figure 9: Schematics BQ25798 Test Board MPPT Solar

8 change log

8.1 Mistakes V1.0

1. no Marking on PCB of min max Voltages.
2. CE Pin not having a resistor to pull LOW to enable chip.
3. too small footprints for soldering.

8.2 V2.0 changes

1. Added support for Dual Power Input
2. Added Backup Mode Support
3. changed charging current to $\approx$ 1A
4. changed Voltage divider for NTC temperature
5. changed PCB layout to accommodate new 2 inputs and outputs
6. added better description to PCB

References

[1] Texas Instruments, *BQ25798 I2C Controlled, 1- to 4-Cell, 5A Buck-Boost Battery Charger with Dual-Input Selector, MPPT for Solar Panels and Fast Backup Mode – Datasheet (Rev. B)*, Jan. 2023, available at: https://www.ti.com/lit/ds/symlink/bq25798.pdf.

[2] LCSC Electronics Co., Ltd., *C51597 — 10 kΩ ±1% 3950 K 0805 NTC Thermistors (FH CMFB103F3950FANT) — Datasheet*, 2025, available at: https://www.lcsc.com/datasheet/C51597.pdf.